REMARKS

Reconsideration of this application is respectfully requested. The following remarks are responsive to the Office Action mailed on May 17, 2000.

Claims 1-20 are pending.

No amendments have been introduced in this response.

In the Office Action mailed May 17, 2000, the Examiner has indicated that applicant's response filed on March 2, 2000 was not fully responsive to the Office Action mailed on September 3, 1999. In particular, the Examiner states:

> The Applicant has not addressed the clear teaching of the Bursky reference that it was known to have read/write/control logic on a memory module. Applicant correctly points out on page 12 of the amendment, last paragraph, that Bursky teaches "one read/write control logic for a plurality of memory modules" in the photo caption of p. 217 and the last two paragraphs of p. 219. However, this teaching of Bursky is directed to an improvement over the prior art which he clearly teaches is a system that has read/write/control logic on each memory module
>
> In the photo caption of p. 217, he states "While most minis duplicate read/write and control electronics for each board of memory DIPs . . . . " (emphasis added) and on p. 219, he writes that ". . . it also means that function duplication is cut back. As a result, the read/write control logic that would have been duplicated on a series of 64-kbyte boards appears just once on the 15x15 in. motherboard . . . ."(emphasis added).
>
> It is this clear teaching of the prior art that is relied on for the rejection. Furthermore, it is this clear teaching that the Applicant has failed to address in his amendment.

Applicant acknowledges the Examiner's reading of the Bursky reference. To address the read/write/control logic of Bursky, applicant respectfully points out the following.

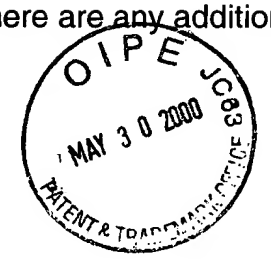
First, the read/write/control logic of Bursky does not teach, disclose, or suggest a system having, *inter alia*, a first memory controller being configured to receive from a system memory controller a first memory transaction in a first format and to convert the first memory transaction into a second memory transaction in a second format as recited in independent claim 1.

Second, the read/write/control logic of Bursky does not teach, disclose, or suggest a system having, *inter alia*, a memory unit with a memory module controller being configured to receive a first memory transaction into a second memory transaction in a second format as recited in independent claim 17.

For the above reasons and the reasons set forth in the response filed on March 2, 2000, applicants respectfully submit that claims 1-20 are patentable over the cited art of record. Accordingly, applicant respectfully submits that claims 1-20 are in condition of allowance.

If the Examiner believes a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 720-8300 x345.

If there are any additional charges, please charge Deposit Account No. 02-2666.



Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Dated: May 25, 2000

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